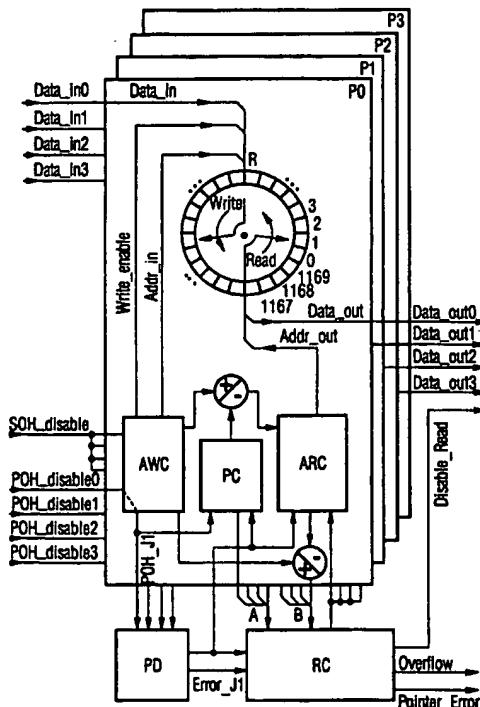




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(54) Titre : PROCEDE POUR CONVERTIR DES SIGNAUX NxSTM-1 EN SIGNAUX STM-N
 (54) Title: METHOD FOR CONVERTING NxSTM-1 SIGNALS INTO STM-N SIGNALS



(57) Abrégé/Abstract:

When SDH signals are transmitted, higher order signals such as STM-N ($N > 1$) signals are transmitted. In order to avoid switching problems with the STM-1 switching networks that have been used until now, the STM-N signals are split into N STM-1 signals according to the known virtual concatenation mode. However, these take different paths in the network which leads to different propagation times. The invention solves this problem by contacting FIFO memory devices at the receiving end with relative addressing so that the useful data stored there can be read out.

Abstract

Method for converting NxSTM-1 signals into STM-N signals

During the transmission of SDH signals, higher-order signals such as STM-N ($N > 1$) signals are transmitted. To prevent circuit switching problems in the STM-1 switching networks hitherto used, the STM-N signals are split into N STM-1 signals in accordance with the known virtual concatenation mode. These signals, however, pass through different paths in the network which leads to different delays. The invention solves these problems by addressing FIFO storage devices with relative addressing at the receiving end in order to read out the payload data stored there.

Figure 3

Description

Method for converting NxSTM-1 signals into STM-N signals

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The invention relates to a method according to the preamble of claim 1.

As a rule, contemporary transmission methods are subdivided into transmission methods which transmit 10 information in accordance with a synchronous transfer mode (STM) or an asynchronous transfer mode (ATM).

The synchronous transfer mode (STM) is based on the transmission of information in SDH (Synchronous Digital Hierarchy) transmission technology. In this 15 technology, the information is transmitted in frames. These are subdivided into a control field (SOH, Section Overhead; POH, Path Overhead) and a container field. In the former, control information relating to the connection is transmitted whilst in the latter, payload 20 is deposited. The payload used can also be ATM cells. These must then be arranged in the frame structure at the beginning of the transmission process and removed again at the receiving end. The control information considered is, for example, information with respect to 25 the security of the transmission, bit errors, circuit failure, clock accuracy, etc.

The control field has two sub-areas SOH and POH. The sub-area designated by SOH has control 30 information with respect to a transmission section (for example between two switching systems) whereas in the sub-area designated by POH, control information is transmitted between two subscribers (end-to-end).

The transmission of information by means of the SDH transmission technology assumes high clock 35 accuracy. If clock inaccuracies occur during the transmission process, for

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example due to delay fluctuations, or if different clock rates are defined due to different situations in different countries, the received containers become displaced beyond the frames. A frame can, therefore, 5 still contain part of the payload of the last container and part of its own container.

In contemporary synchronous transmission systems, STM-1 interfaces are used. An STM-1 interface is physically represented by a connection between two 10 SDH switching systems. The STM-1 interface is thus the basis of the SDH transmission. For this reason, the SDH switching networks arranged in the SDH switching system are currently designed for switching through STM-1 signals in the prior art.

15 In future, however, higher-order signals such as STM-N ($N > 1$) signals are to be transmitted. This results in circuit switching problems in the SDH switching networks hitherto used. A method for bypassing these problems, known in the prior art, is 20 the Virtual Concatenation Mode. This is a standardized method by means of which, for example, STM-4 signals are split into 4 STM-1 signals. During the transmission, 4 STM-1 signals are thus supplied to the receiving switch, switched through and then assembled 25 again to form one STM-4 signal.

In this process, however, the $N \times$ STM-1 signals pass through different paths in the network. Although the $N \times$ STM-1 signals are sent out at the same time, they arrive at different times at the receiving switching 30 center due to different delays. Converting the STM-1 signals into $N \times$ STM-1 signals, however, requires that the STM-1 signals arrive at the same time. In the prior art, storage devices such as, for example, FIFO storage devices are used for recovering the containers in the 35 correct order in order to solve this problem. For this purpose,

the FIFO storage devices must be addressed absolutely which means increased expenditure since, on the one hand, the absolute addresses must always be stored somewhere and on the other hand a +/- area must be 5 reserved. In practice, this is associated with increased control expenditure.

10 The invention is based on the object of demonstrating an approach to have the STM-1 signals sent via different paths which can be regenerated and forwarded in a practical manner at the receiving end.

15 The invention is achieved by the features specified in the characterizing clause on the basis of the features specified in the preamble of claim 1.

20 The advantageous factor in the invention is, in particular, a relative dynamic logic operation between write addresses and read addresses of the FIFO storage devices. This renders superfluous a continuous absolute control of the write and read addresses respectively. Furthermore, such a procedure is associated with a gain in dynamic range during the conversion process.

Advantageous further developments of the invention are specified in the subclaims.

25 In the text which follows, the invention will be explained in greater detail with reference to an exemplary embodiment. In the figures:

Figure 1 shows an SDH container according to the prior art

30 Figure 2 shows the container of an STM-4 interface

Figure 3 shows a circuit arrangement on which the method according to the invention is running

35 Figure 4 shows the reading of the payload from the FIFO storage devices according to the method according to the invention

Figure 5 shows the markers arriving at different times in the FIFO storage devices.

Figure 1 shows the structure of an SDH transmission frame. Accordingly, two SDH frames F_1 , F_2 are shown as examples. The control information is deposited in the control fields SOH, POH. The payload is transmitted in a container CON. According to the exemplary embodiment above, this is intended to be a virtual container VC-4. This means that the payload transmitted here is transmitted at a payload bit rate of 149 Mbit/s.

A frame is built up of a total of 9 rows. The control field SOH has a width of 9 bytes per row. The container CON exhibits a width of 260 bytes per row and the control field POH has 1 byte per row. Overall, this results in a magnitude of 2,430 bytes ($9 \times (9+1+260)$), for one SDH frame, 2340 bytes being provided for transmitting payload.

The start of the container CON in the relevant frame is designated by a marker J_1 . The position of the marker J_1 is stored in a special pointer field H_1 , H_2 , H_3 of the control field SOH which forms a pointer. This pointer points to the position of the marker J_1 . The control information deposited in the control field SOH is always deposited at the same place. The container CON can migrate beyond the frame boundaries F_1 , F_2 due to clock inaccuracies. The same thus also applies to the control field POH. In figure 1, the marker J_1 marks the start of the container CON of the frame F_1 . The start of the container of the frame F_2 is defined by another marker J_1 of frame F_2 . Thus, the payload contained in the container of frame F_1 is also part of frame F_2 beyond the frame boundaries.

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Figure 2 shows the conditions for an STM-4 interface. The STM-4 signals have here been split into 4 STM-1 signals. Here, too, the containers migrate beyond frame boundaries due to clock inaccuracies. The 5 beginning of the individual containers is shown by 4 J_1 pointers belonging to the frames $F_1 \dots F_4$ in figure 2. The origin of this is that, although the 4 STM-1 signals have been sent out at the same time, they have experienced delay differences along the respective 10 paths. For this reason, these signals also have become stored in different storage areas of the FIFO-type buffer stores. Converting the 4 STM-1 signals back into one STM-4 signal requires time-synchronous conversion since only this ensures the STM-4 signal.

15 Figure 3 discloses a circuit arrangement by means of which the restoration of an STM-4 signal from 4 STM-1 signals is achieved. Accordingly, 4 interface devices $P_0 \dots P_3$ are shown. Each of these 4 interface devices $P_0 \dots P_3$ is used at the receiving end to 20 terminate the connecting line via which the STM-1 signal is transmitted in each case. Since the control data transmitted in the control fields SOH, POH are specific to STM-1, this information must be suppressed during the conversion into an STM-4 signal.

25 At the input end, the 4 interface devices $P_0 \dots P_3$ are supplied with the STM-1 signals $Data_in0 \dots Data_in3$. The interface device P_0 is thus supplied with the STM-1 signals $Data_in0$, the interface device P_1 is supplied with the STM-1 signals $Data_in1$, 30 etc. These STM-1 signals are then checked to see whether the incoming information is payload or control information. In the control field SOH, an alignment word is also transmitted to which the frame synchronizes in each case. If this alignment word is 35 received, a signal $SOH_disable$ is activated and supplied to the relevant interface device. The third word in the control field SOH is a pointer which points to the

marker J_1 . If this is detected, a signal $POH_disable$ is activated and this is also supplied to the relevant interface device.

Furthermore, each of the 4 interface devices 5 $P_0 \dots P_3$ has a cyclic circular buffer R . This is constructed as Random Access Memory (RAM) and has the function of a FIFO store. As a rule, this circular buffer R is worth in each case 1170 bytes as one half of a container CON. Furthermore, a counter AWC in which 10 the payload bytes are counted as determined by the state of the signal $SOH_disable$ is in each case provided in each of the interface devices. When both signals $SOH_disable$, $POH_disable$ are inactive, this 15 count is read out and supplied to the circular buffer R via a signal $addr_in$. At the same time, a signal $write_enable$ is supplied. The count of the counter AWC thus reproduces the memory address in the circular buffer R at which the relevant payload bytes are stored. Furthermore, a counter PC which is incremented 20 by the incoming payload bytes on detection of the marker J_1 is provided in each of the 4 interface devices $P_0 \dots P_3$. In a further counter ARC, which is also arranged in each of the 4 interface devices $P_0 \dots P_3$, the address of the circular buffer R under which the 25 payload bytes are read out again is stored as determined by the count of the counter AWC, PC.

The devices PD, RC are used as higher-level devices of the 4 interface devices $P_0 \dots P_3$. The former is a monitoring device which determines whether the 30 markers J_1 of all four interface devices $P_0 \dots P_3$ have been detected. The device RC is a higher-level control logic which controls and monitors the read processes.

In the text which follows, the operation of the circuit will be briefly explained:

The STM-1 signals data_in0...data_in3 are accepted by the relevant interface device. If the 5 signal SOH_disable is inactive, the counter AWC activates a signal write_enable. At the same time, the counter AWC is incremented by the number of incoming payload bytes. The value obtained in this manner is supplied to the circular buffer R via a signal addr_in 10 and is interpreted as address by the buffer. The data data_in are deposited in the circular buffer R as determined by this address. Due to the logical OR operation on the signals SOH_disable, POH_disable (write_enable), only payload is transferred into the 15 circular buffer R. The information stored in the control fields SOH, POH is thus suppressed.

On start-up, the signals POH_J1 of all interface devices P0...P3 are set to "0". If the signaling signal for the marker J1 of the relevant interface device is 20 detected, the counter PC is started by the signal POH_disable. The signal POH_J1 of the corresponding interface device is then set to a logical "1" or "high". As long as the signal POH_J1 assumes the state of logical "1", the payload bytes are counted. If the 25 markers J1 have been received by all interface devices P0...P3, all signals POH_J1 are then set to a logical "1". As a result, the monitoring device PD initiates logic operations and forms the difference between the counts AWC and PC, decremented by 1 and loaded into the 30 counter ARC. The monitoring device PD then sets all signals POH_J1 to 0 for the next cycle. Furthermore, if the counts of the counters AWC and ARC are equal, the read process is stopped in all interface devices and a signal disable_read is generated because there is no 35 payload in the circular buffer R

in at least one of the interface devices $P_0 \dots P_3$.

In detail, the following procedure is adopted:

The counts of counters AWC and PC are determined. The difference between the two counts is 5 decremented by 1 and the result is stored in the counter ARC. At the instant at which all markers J_1 have arrived, the relative delay difference of the STM-1 signals with respect to the STM-1 signals which have arrived last is thus given in the counter PC.

10 The counters ARC of all interface devices are then triggered to transfer the content to the circular buffer R via in each case one signal addr_out. The latter interprets this value as an address. The data stored under this address are read out and forwarded as 15 STM-4 signal as output data data_out.

The corresponding conditions are reproduced in figure 4. Accordingly, the 4 cyclic circular buffers R of the 4 interface devices $R(P_0) \dots R(P_3)$ are shown. As a 20 last marker, marker J_1 of the interface devices P_1 has arrived, for example. All counters are then stopped. Subsequently, the relative address to the markers J_1 which are stored in the remaining 3 interface devices is then formed. In the case of the interface devices $R(P_0)$ the difference is 6 payload bytes. In the case of 25 the interface device P_2 , the difference is 8 payload bytes and in the case of the interface device P_3 , the difference is 17 payload bytes. Triggering the higher-level logic device RC, the payload is read out and supplied to an STM-4 frame FR which regenerates 1 STM-4 30 signal from the 4 STM-1 signals.

The precondition for this method is that the markers J_1 of all STM-1 signals arrive within a half VC-4 period. The corresponding conditions are shown for the example of 4 STM-1 signals in figure 2. The markers 5 J_1 are placed within the VC-4 period. For this reason, the interface circuits can synchronize without additional signal evaluation. For example, marker J_1 of frame F_3 of interface device P_3 arrives first, for example, as described for figure 2. The counter PC is 10 then started and counts up to 1170. If no further markers J_1 of the remaining containers CON are detected until then, all counters PC and all signals POH_J_1 are reset and synchronization recommences correctly with marker J_1 of frame F_1 at the next cycle.

15 According to the present exemplary embodiment, it has been assumed that the magnitude of the delay differences is smaller than one half container period of a virtual VC-4 container. However, delay differences greater than one half container period of a virtual 20 VC-4 container can also be treated with a modification of the method.

The interface device according to figure 3 can still synchronize if the payload in the container is structured. In this case, the circular buffer R must be 25 enlarged in accordance with the greatest delay to be expected. The corresponding conditions are shown in figure 5. This is the case, for example, if the payload consists of ATM cells, frame relay or TCP/IP data. Because of such transmission formats, synchronization 30 can be carried out because error-free transmission is detected by the control field SOH and in this case the header of the cell is detected and evaluated by an additional payload synchronization circuit corresponding to the transmission format. The 35 synchronization circuit is designated by HSC in figure 5. The synchronization can be restored by

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combining the pointers of 2 or more VC-4 containers (4 pointers in the case of STM-4) until the payload synchronization circuit HSC acquires lock. The combination can be obtained from a simple addition of 5 2340 bytes in the counting devices of the counters ARC - triggered by a device J_1 CL (J_1 combining logic) since, when a number of markers J_1 is found, the frame to which this marker belongs cannot be reliably detected. The difference between 2 markers J_1 of the 10 same interface device is 2340 payload bytes. After the payload synchronization circuit HSC has acquired lock, the markers J_1 will not be combined because only jumps of 3 bytes are allowed according to the SDH standard, unless the system is re-initialized.

Patent claims

1. A method for converting NxSTM-1 signals into STM-N signals, comprising
 - 5 a multiplicity (N) of STM-1 signals (data_in0...data_inN) which in each case have a first and second control field (SOH, POH) and a payload field (CON) filled with payload, the beginning of which is defined by a marker (J₁) and comprising a multiplicity (N) of interface devices (P₀...P_N) which in each case have a store (R) and which are used for accommodating the multiplicity (N) of STM-1 signals (data_in0...data_inN), characterized in that
 - 15 the payload of the multiplicity (N) of STM-1 signals is stored in a cyclic order in the store (R) of the in each case associated interface device (P₀...P_N) at a write address corresponding to the number of payload data which have arrived,
 - 20 a relative address is formed with respect to the markers (J₁) which have arrived until then, on the basis of the marker (J₁) which has arrived last, and at the relative address formed in this manner, the payload is removed again from the stores (R) of the in
 - 25 each case associated interface device (P₀...P_N) in the same cyclic order as during the write process and is supplied to an STM-N frame (FR) as output data (data_out0...data_outN).
2. The method as claimed in claim 1,
 - 30 characterized in that, the write address in the store (R) is formed by incrementing in a first counting device (AWC) as determined by the number of payload data that have arrived, until the first control field (SOH) or the
 - 35 second control field (POH) is detected, and the count of the first counting device (AWC) is transferred to the store (R).

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3. The method as claimed in claim 1,
characterized in that,

the payload data are counted in a second counting
device (PC) from the instant where the second control
5 field (POH) is detected until the time where all
markers (J_1) have arrived, and then the difference
between the counts of the first and second counting
device (AWC, PC) is formed, which is further
decremented by 1, and the value calculated in this
10 manner is transferred as read address to a third
counting device (ARC) at which the payload stored in
the store (R) is removed.

4. The method as claimed in one of claims 1 to 3,
characterized in that,

15 the store (R) is constructed as a cyclic random-access
circular buffer.

5. The method as claimed in one of claims 1 to 4,
characterized in that,

the interface devices ($P_0 \dots P_N$) are synchronized within
20 one half period of a VC-4 container (CON).

6. The method as claimed in one of claims 1 to 4,
characterized in that,

the interface devices ($P_0 \dots P_N$) are synchronized outside
the half period of a VC-4 container (CON) by combining
25 the pointers of at least two VC-4 containers until a
synchronization circuit (HSC) which follows the
interface devices ($P_0 \dots P_N$) and determines structured
payload data acquires lock.

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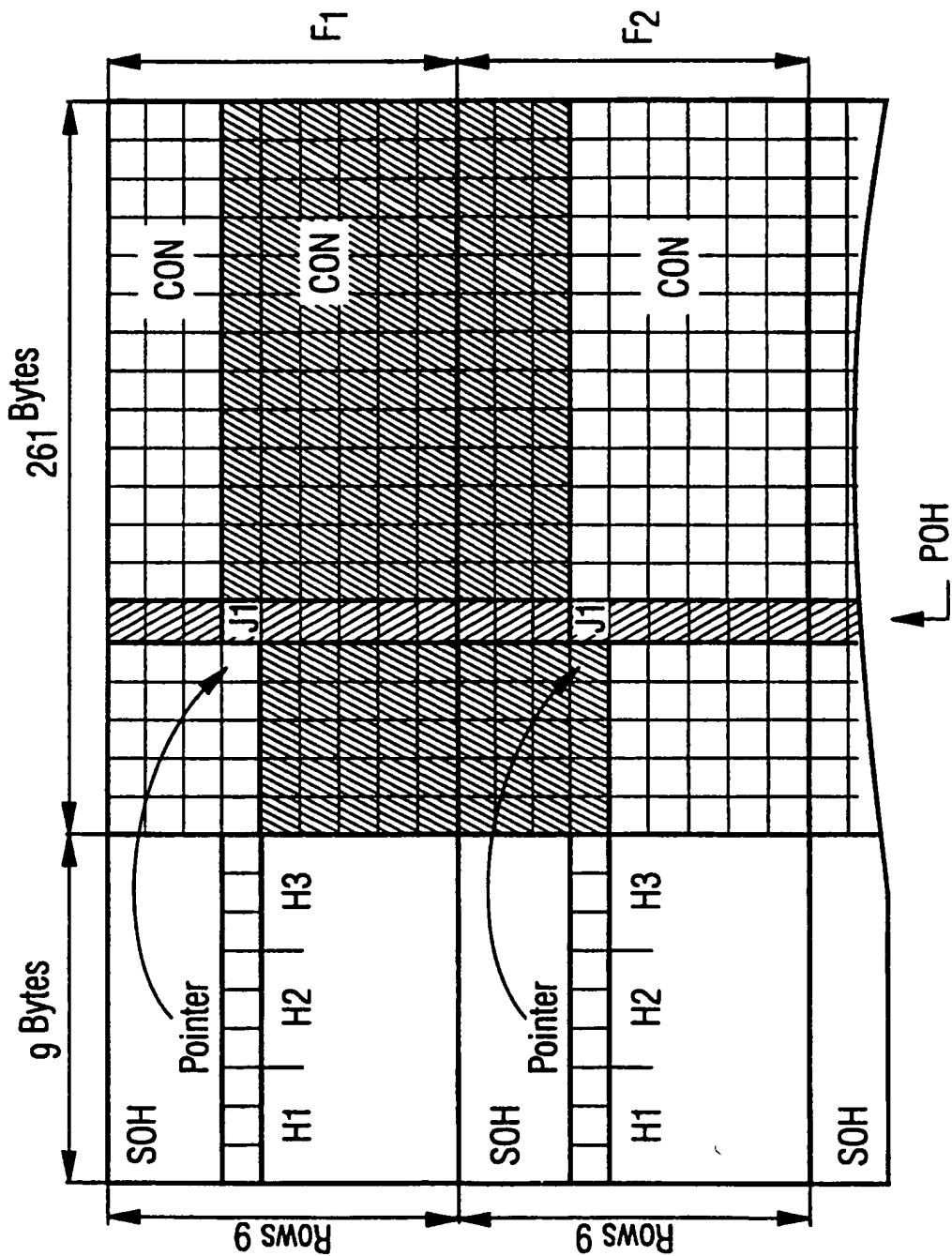


FIG 1

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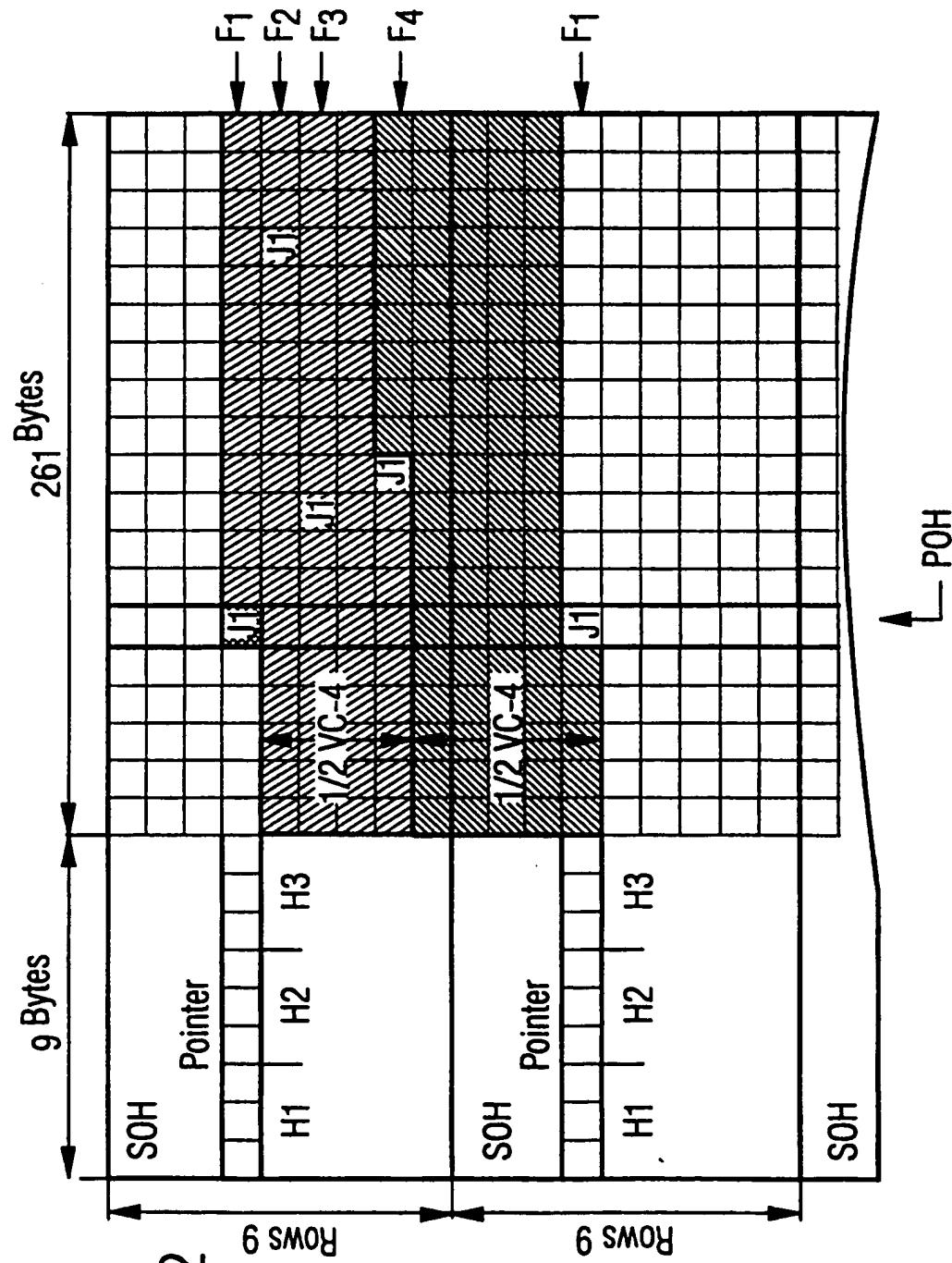
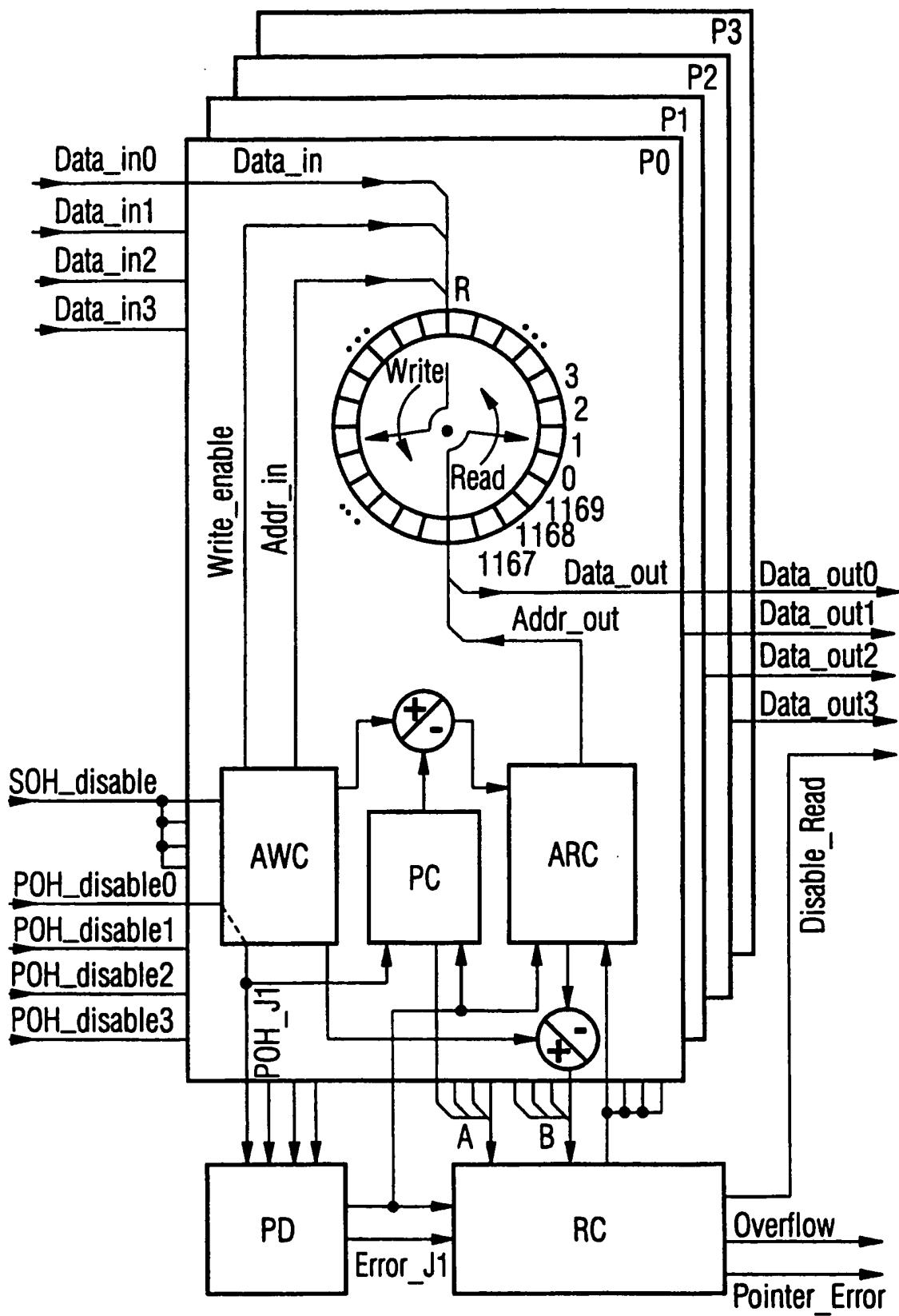


FIG 2

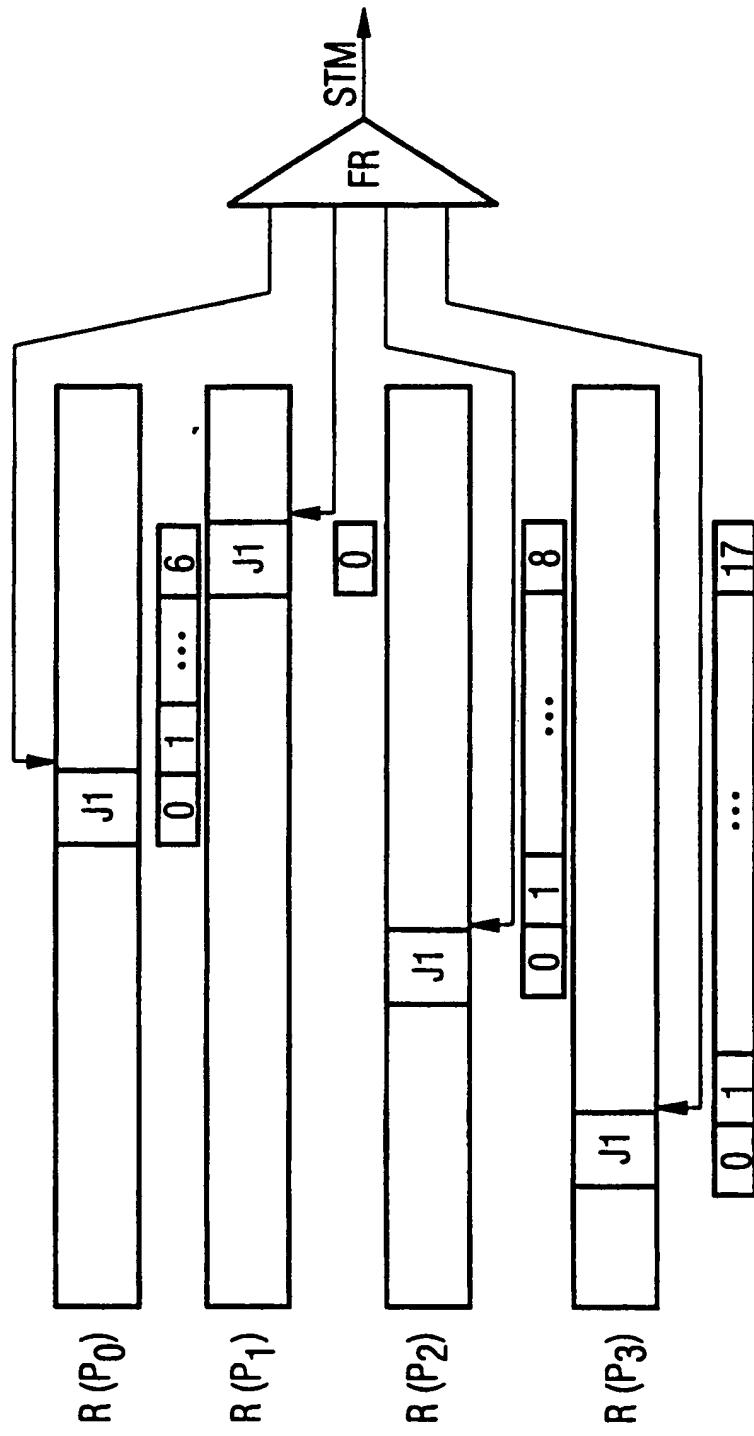
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FIG 3



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FIG 4



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FIG 5

